Single Chip OQPSK Modem Appropriate for Wireless Burst Data Communications

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Abstract

A single chip all-digital modem appropriate for Time Division Multiple Access (TDMA) transmission is presented. Using a fully parallel and pipelined hardwired VLSI architecture, this Application Specific Signal Processor (ASSP) implements the baseband transmitter and receiver functions for Offset Differential QPSK at bit rates up to 8Mbit/s. This includes data encoding, pulse shaping, burst formation, non-coherent demodulation, clock recovery, soft decision decoding and an accurate burst detection circuit. The modem can operate either in a linear receiver or in a limiter receiver architecture without performance degradation. Although developed to accommodate a symmetric point-to-multipoint PCM TDMA wireless access system, this highly flexible device can also provide an asymmetric TDMA reverse link solution.

1. Introduction

In the last few years a large number of wireless communication systems transmitting data in a burst by burst manner have been deployed that include fixed and mobile communication systems within a large spectrum of different modulation formats, topologies, capacities and access protocols. Among them, in wireless TDMA systems a significant overhead is usually required for allowing reliable recovery of the received signal parameters such as the carrier frequency and phase, the transmitter clock and the signal amplitude. Minimisation of this overhead implies better exploitation of the expensive bandwidth resource. A number of systems addressing solutions to this composite problem have been studied, prototyped or even deployed in the last few years providing an answer to the emerging demand of wireless fixed or mobile telephony and internet access services [1][2][3].

Although the system presented in this paper has been developed to accommodate a symmetric point-to-multipoint PCM TDMA wireless access system, it follows the paradigm of mobile telephony, where non coherent demodulation is used. In particular, employing Offset Differential QPSK with non-coherent demodulation and an extremely fast clock recovery technique offers two advantages: First, short guard time between the data bursts and short preamble length are obtained which allow for short data burst and consequently small latency time at system level. Second, the system behaves very well when operating in the presence of large carrier frequency deviations, microwave synthesizer phase noise or microphonics, as well as in fast fading channel conditions, especially if a hard limiter receiver architecture is used. Both of the above features are further aided by a careful burst shaping logic, in

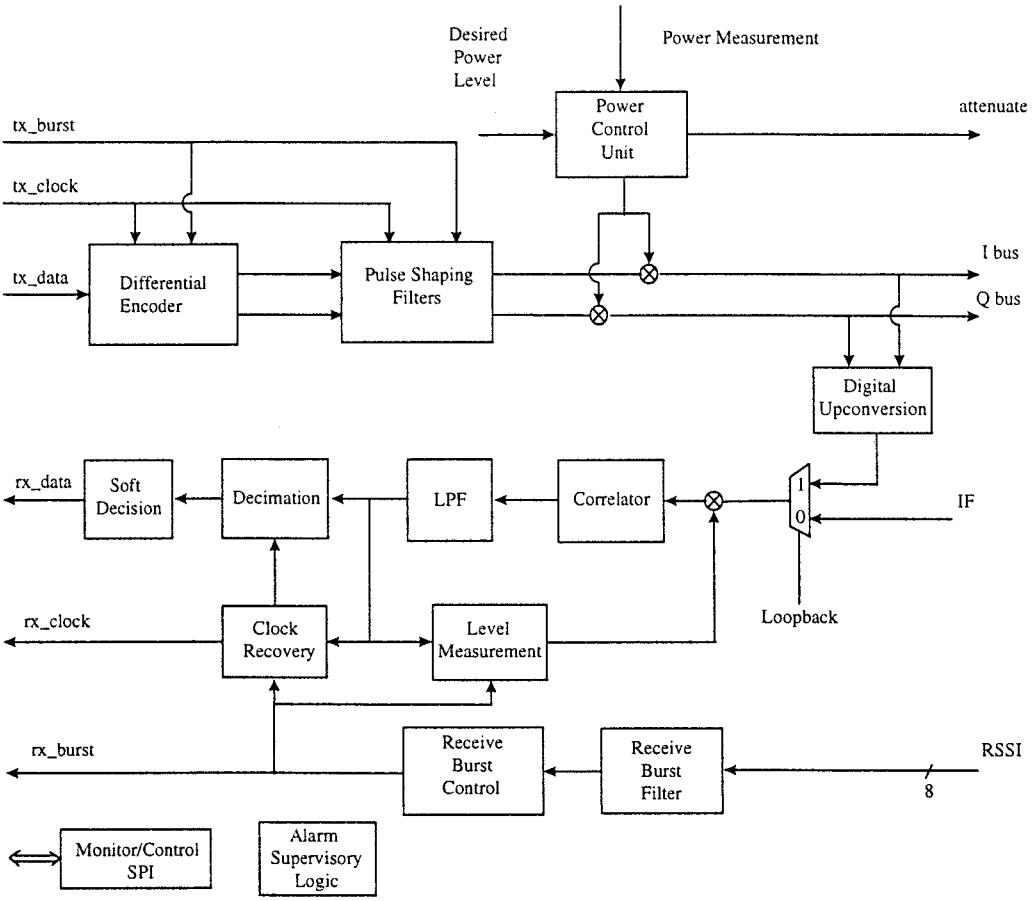

Figure 1: ODQPSK ASSP functional block diagram

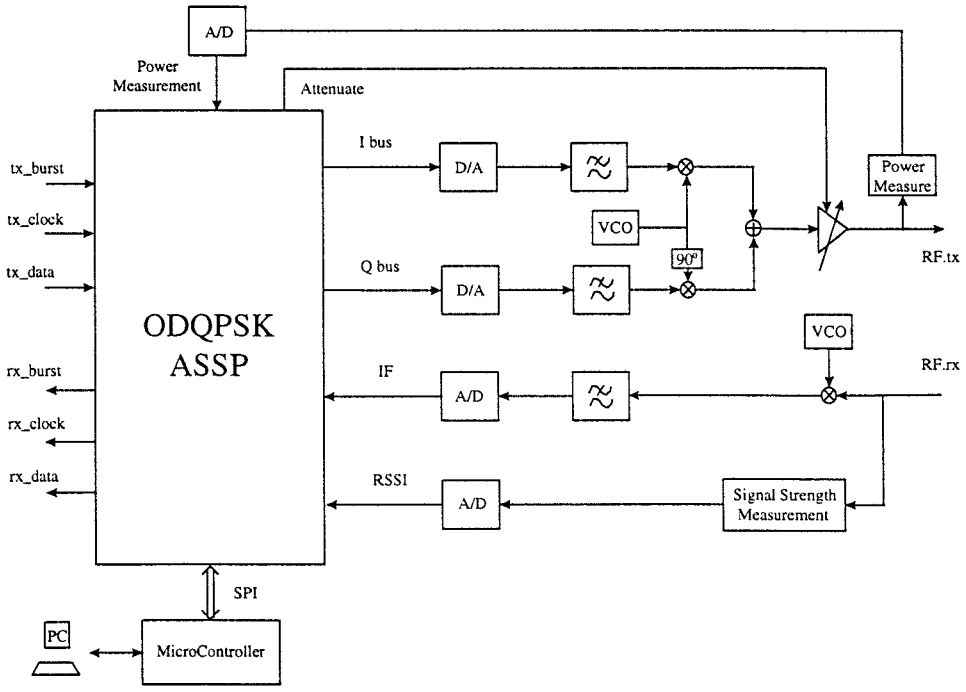

Figure 2: Application note

combination with a time accurate carrier detector. A detailed presentation of these modules along with a flexible peripheral circuitry shown in Figures 1 and 2 follows.

2. Transmitter

The transmitter circuitry consists of the differential encoder, the pulse shaping filters and power control unit and a pair of gain elements as shown in Figure 1. The three binary input signals *tx_data*, *tx_clock* and *tx_burst* represent respectively the data sequence to be transmitted, the transmitter clock and a control signal signifying the boundaries of the data bursts. The transmitter output consists of two baseband signal busses *I_bus*, *Q_bus*.

Following the encoding rule of Kaleh [4],[5], the differential encoder produces a complex symbol b_k at time instant k on the basis of the input antipodal symbol a_k and the output complex symbol b_{k-1} according to the formula:

$$b_k = j a_k b_{k-1},$$

where a_k and b_k take values in the sets $\{-1, 1\}$ and $\{-1, 1, -j, j\}$ respectively.

The pulse shaping filters are full raised cosine filters with a rolloff factor equal to one. These filters have compact impulse time response appropriate for minimising the inter-burst interference, thus allowing minimal guard time intervals between consequent bursts.

The Power Control Unit (PCU) enables accurate transmit power selection and ensures thermal stability and repetitiveness of the system performance. The PCU produces a fine tuning gain factor controlling the digital gain of the busses *I_bus* and *Q_bus* as shown in Figure 1. It also produces an attenuation code for coarse scaling the transmitter radio signal as shown in Figure 2. A power measure block extracts the envelop of the transmitted signal, that is sampled and fed to the PCU. The PCU is responsible for using only valid power measurements, that is avoiding guard time intervals where zero power is transmitted.

3. Receiver Data path

The receiver data path consists of the demodulator, the Automatic Level Control (ALC) and the decision making circuitry, while the receiver input consists of an Intermediate Frequency (IF) signal.

The demodulator is implemented by a complex correlator followed by lowpass filtering [6] and it is preceded by a programmable delay. The latter serves the purpose of aligning the receiver IF signal with a received power envelop signal discussed in the following section. This demodulator structure is shown in Figure 3 and the associated eye diagrams are shown in Figures 4 and 5.

The ALC is responsible for keeping the filter output fixed to some parameter specified level invariable of temperature changes and ageing. It is implemented by a Level Measurement Unit (LMU) and a digital gain feeding back the correlator input. For the case of burst operation, active *rx_burst* is required for the LMU to take measurements.

Soft decoding and equalisation is carried out by a Viterbi algorithm [6].

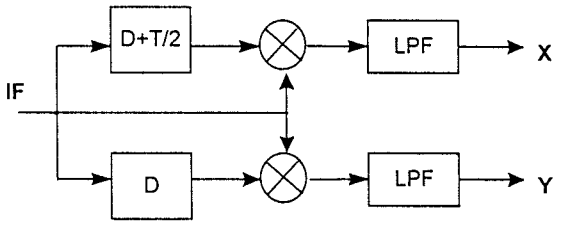

Figure 3: DOQPSK demodulator

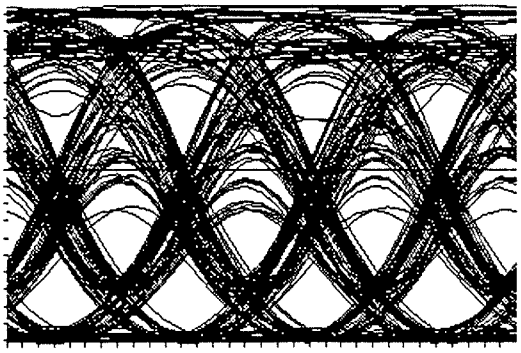

Figure 4: X-eye diagram

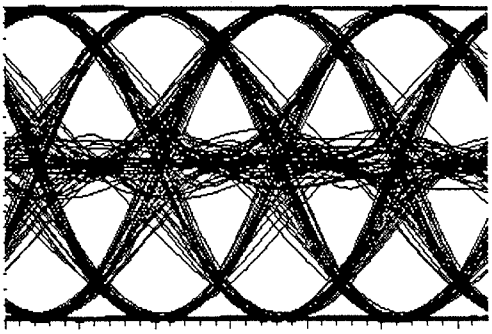

Figure 5: Y-eye diagram

4. Burst Detector

A burst recovery circuit receives as input a receive signal strength indicator (RSSI) providing the envelop of the received radio signal and it consists of two stages. The first one is a smoothing stage that captures the analogue features of the envelop signal and the second one captures the burst and frame structure. In Figure 1, these are labelled as Receive Burst Filter and Receive Burst Control respectively. The overall process is very flexible and provides a very low jitter burst detect signal. In particular, the produced burst detect signal *rx_burst* has a jitter as low as two symbols for an operational dynamic range of 65dB.

5. Clock Recovery

The clock recovery circuit implements an ultra fast convergent algorithm based on the derivative extrema of the incoming waveform. The block diagram of this clock recovery algorithm is shown in Figure 6. When operating in burst mode, the clock recovery circuit gets reset on a burst by burst basis, which implies a maximum degree of flexibility and reliability. The algorithm requires a preamble as short as three symbols, while it offers no performance degradation compared to the continuous mode operation.

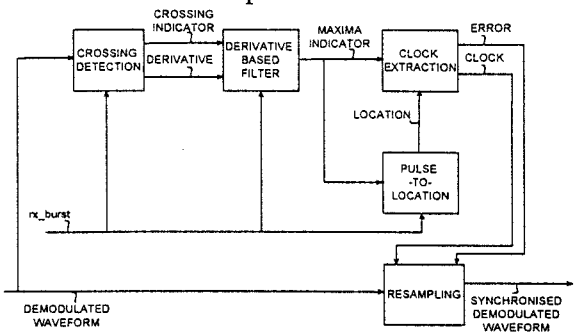

Figure 6: Clock recovery block diagram

6. Test and Monitor Circuitry

Provision for a loopback operation mode has also been taken. The purpose of the loopback mode of operation is to provide a simple and efficient functional test covering most of the transmitter and receiver modules inside the ASSP without the interception of the external IF/RF transmission and reception circuitry. The transmitter output is a baseband I/Q signal, while the receiver needs an input representing an Intermediate Frequency (IF). An internal digital up-conversion circuit is used in order to emulate the external system. The loopback mode may be used in conjunction with both continuous and burst mode operation.

Finally, a set of tools for monitor, control and testing including a powerful monitor/control panel and interface logic for a PC, a complete set of alarm supervisory points, programmable system parameters and test points, pattern generation and loopback logic are provided. With these tools the system parameters (such as burst length, decision making thresholds, burst recovery features etc.) can easily be tested and modified.

7. Implementation Issues and Conclusion

The ODQPSK modem described in this paper, covered by four pending patents, has been used for implementing the physical layer of a point-to-multipoint time division multiple access (TDMA) system. This system is able to accommodate transmission rates up to 8Mbit/sec. The resulted SNR-BER curve is shown in Figure 7. This is compared to simulated single-branch demodulators using either hard decoding [4] or 2-state soft decoding [5]. We observe a 3.5dB improvement with respect to the first one and a 2dB improvement with respect to the second one. The SNR-BER performance curve of our ODQPSK receiver is marginally better than the one of non-coherently demodulated $\pi/4$-DQPSK. In this respect, the presented ODQPSK modem shares a combination of advantages enjoyed by GMSK systems, such as using power efficient low output back-off or class C power amplifiers with band-limited transmission and the advantage of efficient reception offered by $\pi/4$-DQPSK systems.

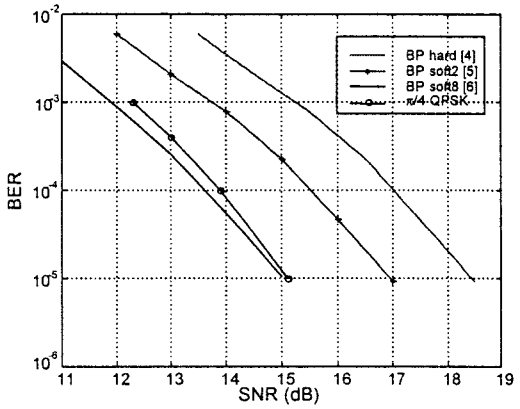

Figure 7: SNR-BER plots

The ASIC has been manufactured on a 0.6 μm technology in a 128 PQFP packaging consuming 600mW peak.

Experiments that are not reported in this brief presentation show improved robustness against co-channel and adjacent channel interferences compared to other ODQPSK and $\pi/4$-DQPSK receivers.

References

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